REMARKS

Claims 1, 7, 9-12, 15, 17-19, 21-22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are currently pending, of which claims 1, 9, 15 and 129 are the pending independent claims. Claims 4, 29, 30 and 115 were previously withdrawn, and claims 2-3, 5-6, 8, 13-14, 16, 20, 23-24, 26, 28, 31-90, 92-95, 100 and 104-107 were previously cancelled without prejudice. No claims are added or cancelled herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

Claim Rejections

Claims 1, 7, 9-12, 15, 17-19, 21-22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lin (U.S. Patent No. 6,303,423) (hereinafter, "Lin") in view of Nakanishi (U.S. Patent No. 6,921,980) (hereinafter "Nakanishi"). Reconsideration and withdrawal of these claim rejections are respectfully requested.

Claim 1

Independent Claim 1 is drawn to an integrated circuit chip comprising, a semiconductor substrate, a transistor in and on the semiconductor substrate, multiple metal and dielectric layers over the semiconductor substrate, a first contact pad over said semiconductor substrate, a second contact pad over said semiconductor substrate, and a passivation layer over the multiple metal and dielectric layers, wherein the passivation layer comprises a nitride. A first opening in the passivation layer is over a first contact point of the first contact pad, and the first contact point is at a bottom of the first opening. A second opening in the passivation layer is over a second contact point of the second contact pad, and the second contact point is at a bottom of the second opening. The chip also includes a power metal structure over the passivation layer and on the first contact point, wherein the power metal structure is connected to the first contact point through the first opening. The power metal structure comprises a copper layer. The power metal structure has a first region not vertically over the first opening configured to be wirebonded thereto for connection made to a next level of packaging. The chip also includes a ground metal structure over the passivation layer and on the second contact point, wherein the ground metal structure is connected to the second contact point through the second opening. The ground metal

structure comprises a copper layer. The ground metal structure has a second region configured to be wirebonded thereto for connection made to the next level of packaging. The chip also includes a capacitor over the passivation layer and the power and ground metal structures. The capacitor has a first terminal and a second terminal. The first terminal is vertically over the first contact point. The chip also includes a first solder joint between the first terminal of the capacitor and the power metal structure, wherein the first solder joint connects the first terminal to the power metal structure, and a second solder joint between the second terminal of the capacitor and the ground metal structure, wherein the second solder joint connects the second terminal to the ground metal structure.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing combination of features of claim 1.

The Office Action again asserts that Lin teaches, with reference to Fig. 10 copied below, a circuit chip having a substrate 10 with first and second contact pads 16, and a passivation layer 18, wherein the Office Action identifies the first contact point as on the left pad 16 and the second contact point as on the right pad 16. The Office Action again further identifies "a power metal structure (structure directly above 16 shown on the right side, see Col. 8, lines 21-24)" and "a ground metal structure (structure directly above 16 shown on the left side, see Col. 8, lines 21-24) over said passivation layer (18) and on said second contact point" wherein Lin teaches in col. 8, lines 21-24 that "A pad can, for instance, be used as a flip chip pad. Other pads can be used for power distribution or as a ground or signal bus." The Office Action also again asserts that Lin teaches a capacitor 54 with "a first solder joint (joint corresponding to one of the 52) vertically over said first contact point (as explained above, noting that at least part of 52 is vertically over 16, as seen in Figure 10) and between a first terminal of said capacitor (first terminal of capacitor 54 that is just above first solder contact and which bonds with the first solder contact forming an electrical connection to the corresponding capacitor for input/output) and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure." See Office Action, p. 2, line 8 to p. 5, line 18.

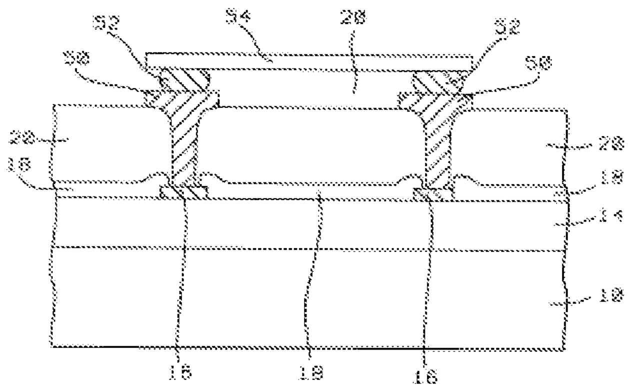
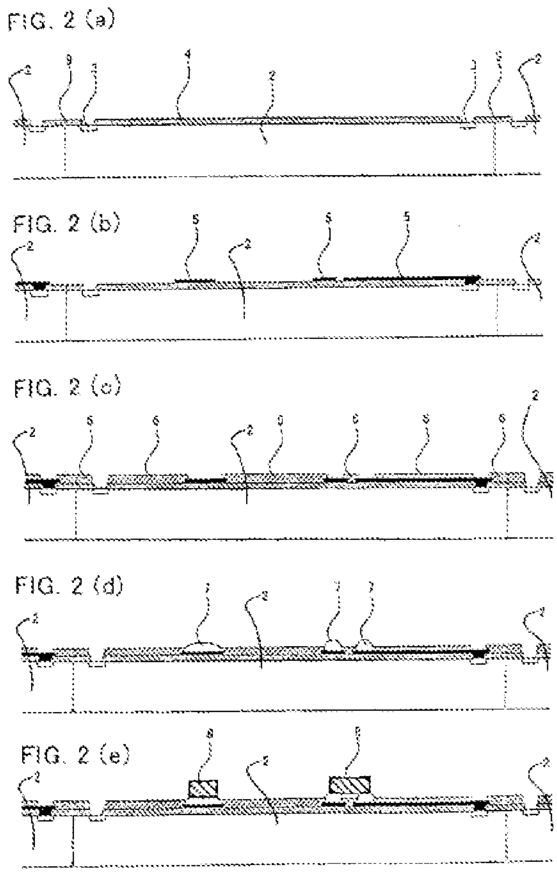


FIG. 10

Fig. 10 from Lin.

The Office Action admits that Lin fails to teach a region used to wirebond thereto but asserts that Nakanishi teaches, with respect to Figs. 2(a)-2(e) and 3(a) copied below, "a capacitor (8) mounted to a metallization structure comprising a copper layer (Col. 4, lines 58-63), which can server as a power or ground structure), wherein the metallization structure has a second region used to be wirebonded (by wirebonds 12) thereto" and that "It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi so that said power metal structure and said ground metal structure has a first region and a second region, respectively, used to be wirebonded thereto for connection made to a next of packaging. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing routing for interconnects to <u>contact pads that are closer to the periphery of the semiconductor substrate</u> (compared to the capacitor, thus allowing flexibility of <u>placing the capacitor in a central location on the semiconductor substrate</u>, as shown in Figure 3b of Nakanishi), while still being able to connect to the ground or power of next level of packaging without excessive wirebond length and a high electrical conductivity metal, like copper, which improves electrical performance and which allows long interconnect length, to connect to next level of packaging." [emphasis added] *See* Office Action, p. 5, line 17 to p. 6, line 8.



Figs. 2(a)-2(e) from Nakanishi

FIG. 3 (a)

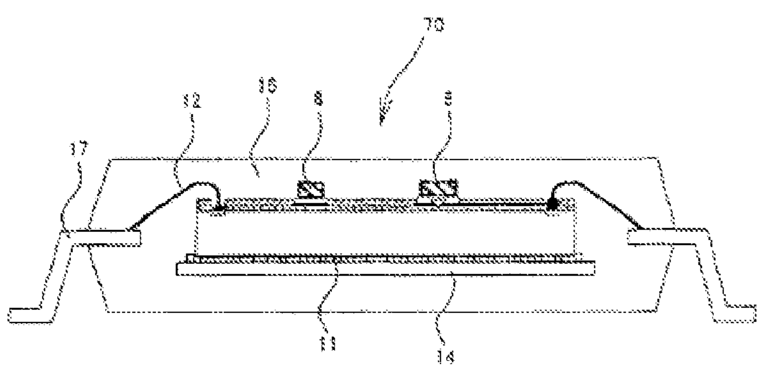


Fig. 3(a) from Nakanishi

As mentioned in Applicants' previous Response, the instant application is drawn to a configuration, with reference to Fig. 3 copied below, where a discrete decoupling capacitor 38 having first and second terminals 34 is mounted over the passivation layer 18 with a first terminal 34 <u>directly over</u> the Vdd metal segment in the top layer of metal underlying passivation layer 18. "The wirebond on the left 26 is connected to Vdd and the wirebond on the right 28 is connected to Vss." *See* the instant application, p. 8, lines 17-18. The location of the decoupling capacitor 38 between the wirebond 26 and the Vdd pad provides improved decoupling by minimizing the inductance and resistance between the capacitor 38 and the Vdd pad, and the use of a discrete capacitor enables provisions of a larger capacitance that can be provided by a capacitor fabricated on the chip. Thus, the position of the capacitor terminal over the Vdd metal segment while the wirebond pad is further away, i.e. <u>not</u> vertically over the Vdd metal segment <u>but still connected to the Vdd metal segment through the thick copper layer that is over the passivation</u>, is important to the function.

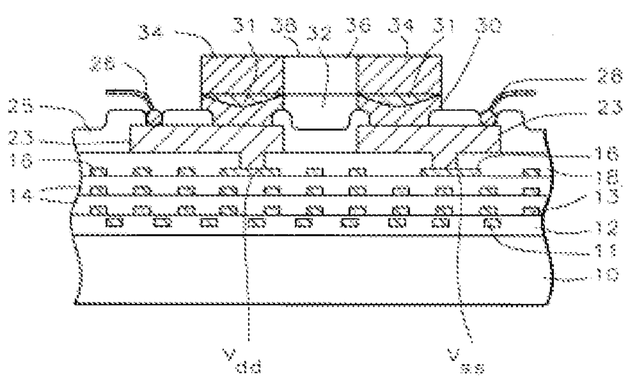


FIG 3

Fig. 3 from the instant application.

Applicant disagrees with the Office Action's characterization of the teachings of Nakanishi. Nakanishi is seen to teach that <u>wires 12 are connected directly to or directly over pads 3</u> as shown in Figs. 2(e) and 3(a) and that the discrete components are separated from the pads 3 by wiring traces 5. Thus, the applying the teachings of Nakanishi to the chip of Lin would connect the bond wire to the contact plug 50 that is vertically over the contact pad 16 and

would then offset the discrete component 54 from the contact plug 50. Thus, the combination of Lin and Nakanishi does not produce a chip with the feature that "*a first opening in said passivation layer is over a first contact point of said first contact pad*... [and] *a power metal structure over said passivation layer*… [that] *has a first region not vertically over said first opening configured to be wirebonded thereto for connection made to a next level of packaging; a capacitor over said passivation layer and said power and ground metal structures, said capacitor comprising a first terminal and a second terminal, said first terminal vertically over said first contact point*" as recited in claim 1.

Furthermore, Nakanishi is seen to teach that "The wiring traces 5 are formed by the following steps. First, on the lower insulating film 4 and the electrode pads 3, i.e., on the entire surfaces of the semiconductor chips 2, titanium tungsten (TiW) and copper (Cu) are deposited sequentially by sputtering to have a thickness of 0.1μm, respectively. Then, a photosensitive resist of 10μm thick is formed on the thus deposited copper, and then light exposure and development are carried out by using a mask to form grooves (not shown) in which the wiring traces 5 will be formed. Then, copper is deposited in the grooves in a thickness of 5 μm by electrolysis plating, the photosensitive resist is chemically peeled off, and the exposed films of TiW and Cu formed by sputtering are removed. Thus, the isolated wiring traces 5 of copper are formed." *See* Nakanishi, col. 4, lines 29-41. Nakanishi also is seen to teach that "In the semiconductor package 70 shown in FIG. 3(a), the semiconductor chip 2 on which the discrete electronic components 8 have been mounted is fixed onto a region called a die pad 14 with a die attachment member 11 such as silver paste. They are encapsulated in an epoxy resin 16 and the electrode pads are electrically connected with lead terminals 17 via wires 12, respectively." *See* Nakanishi, col. 5, lines 15-21. Applicants submit that wire 12 cannot be bonded to wire trace 5 since, as pointed out in the instant application, "If a wirebond is to be made to copper, a layer of nickel, then a layer of gold are formed over the copper." *See* the instant application, p. 12, lines 1-2. Nakanishi is seen to be silent as to any further metal layers over the traces 5, and therefore the wiring traces 5 cannot form the power metal structure of claim 1 as a wirebond cannot be made to the bare copper of the wiring traces 5. Wires 12 can be bonded only to the pads 3 from which the sputtered TiW and Cu were removed, i.e. not under wiring traces 5. Pads 3 are under the passivation layer and, for reasons presented above, the external wires 12 and

wiring traces 5 must connect to different pads 3. Accordingly, Nakanishi teaches away from "*a power metal structure over said passivation layer and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening, wherein said power metal structure comprises a copper layer, wherein said power metal structure has a first region not vertically over said first opening configured to be wirebonded thereto for connection made to a next level of packaging*" as recited in claim 1.

In response to Applicants arguments, the current Office Action includes the remarks that "applicant argues that 'applying the teachings of Nakanishi to the chip of Lin would connect the bond wire to the contact plug 50 that is vertically over the contact pad 16 and would then offset the discrete component 54 form the contact plug 50' (see page 17, last paragraph). This argument is not persuasive. Referring to Figures 2 and 3 of Nakanishi, it suggests keeping the discrete component (54 of Figure 10 of Lin or its equivalent 8 of Figure 2e and 3 of Nakanishi) as is, but extending a part of the metallization towards a periphery of the device so as to provide an additional pad that is electrically connected to the passive component but being closer to periphery of the device, is suitable for wire bonding. In implementing this, there is no need to 'offset the discrete component 54' (as argued by the applicant). Applicant also argues that Nakanishi forms 'isolated wiring traces 5 of copper' (see page 18, 2nd paragraph, especially last sentence). It appears that applicant is alleging that wiring traces 5 of Nakanishi are not capable of interconnecting components or component pads. This argument is not persuasive as it is well known in the art that the very function of traces in this context is to achieve interconnection. Even if a trace is not connected to other traces, it can still interconnect two components when the respective components are connected, for example, one at each end of the trace, thus enabling interconnection of components." See Office Action, p.23, line 14 to p. 24, line 12.

Applicants respectfully disagree with the foregoing comments and submit that the Examiner is attempting to re-design Applicants invention in order to force to references together that otherwise teach away from each other. The argument in the Office Action that "extending a part of the metallization towards a periphery of the device so as to provide an additional pad that is electrically connected to the passive component but being closer to periphery of the device, is suitable for wire bonding" such that "there is no need to 'offset the discrete component 54" is not

supported by the applied references. In this regard, the resulting structure suggested by the Examiner would not be Applicants invention.

As mentioned above, the location of the decoupling capacitor 38 between the wirebond 26 and the Vdd pad provides improved decoupling by minimizing the inductance and resistance between the capacitor 38 and the Vdd pad, and the use of a discrete capacitor enables provisions of a larger capacitance that can be provided by a capacitor fabricated on the chip. Thus, the position of the capacitor terminal over the Vdd metal segment while the wirebond pad is further away, i.e. not vertically over the Vdd metal segment but still connected to the Vdd metal segment through the thick copper layer that is over the passivation, is important to the function.

The Office Action's proposed structure would result in the position of the capacitor terminal being offset from the Vdd metal segment, and an extended metallization to provide an additional pad, which is not recited in Applicants' Claim 1. Accordingly, Applicants submit that the contrived structure proposed in the Office Action is not supported by the applied references, but is instead clearly based on impermissible hindsight in view of Applicants' own disclosure.

The Office Action also sets forth the comment that "On page 18, last paragraph, applicant argues that 'Wires 12 can be bonded only to the pads 3 from which the sputtered TiW and Cu were removed". This argument is not clear. Applicant's claim only recites 'configured to be wirebonded thereto for connection made to said next level of packaging' and this has been addressed in view of Nakanishi which also teaches wirebonds and as such teaches regions that are configured to be wirebonded thereto for connection made to said next level of packaging - if this was not the case, wirebonding shown in Nakanishi would not be possible." See Office Action, p. 25, lines 1-8. However, this response in the Office Action misses the point that Nakanishi's wires 12 can only be bonded only to the pads 3 because wires 12 cannot be bonded to wire trace 5 since, in the instant application, "If a wirebond is to be made to copper, a layer of nickel, then a layer of gold are formed over the copper", but Nakanishi is silent as to any further metal layers over the traces 5 and does not teach any such metal layers that would allow wires 12 to be bonded to trace 5. To account for this glaring deficiency of the Office Action's proposed structure, the Office Action simply states that Nakanishi has wirebonds and therefore must somehow teach the specific elements of Applicants Claim 1. Again, Applicants submit that this

position is not supported by the applied references, but is instead clearly based on impermissible hindsight in view of Applicants' own disclosure.

In view of the above, the combination of Lin and Nakanishi fails to disclose or make obvious a chip having the specific limitations recited in Claim 1, and reconsideration and withdrawal of the rejection of Claim 1 are respectfully requested. In this regard, for at least the above reasons discussed with regard to Claim 1, independent Claims 9, 15 and 129 are also believed to be allowable over the applied references and reconsideration and withdrawal of the rejections of Claim 9, 15 and 129 are also respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the remarks set forth herein, Applicant submits that the application is in condition for allowance and respectfully requests a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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